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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,387	12/04/2003	Kevin L. Robinson	LMC-34	7745
45722	7590	04/12/2006	EXAMINER	
PLEVY & HOWARD, P.C. P.O. BOX 226 FORT WASHINGTON, PA 19034			LUU, CHUONG A	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary

Application No.

10/727,387

Applicant(s)

ROBINSON, KEVIN L.

Examiner

Chuong A. Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 February 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 1 and 2 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

WITHDRAWN

The indicated finality of claims 3-19 is withdrawn in view of the newly discovered reference(s) to Higashisaka (U.S. 5,030,852) and Newman et al. (U.S. 5,705,940).

Rejections based on the newly cited reference(s) follow.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 3, 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Higashisaka (U.S. 5,030,852).

Higashisaka discloses a MESFET logic circuit with

(3); (10) a first block comprising an enhancement mode PHEMT transistor on a substrate;

a second block comprising a depletion mode PHEMT transistor on the substrate, the second block operatively connected to the first block (see Figures 1-2);

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a third block comprising a power PHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block; an analog input in communication with at least one of the first block, the second block (see column 7, lines 21-25 and column 9, lines 20-27. Figures 1-2);

(7) an enhancement mode PHEMT device, a depletion mode PHEMT device on a single substrate (see column 7, lines 21-25 and column 9, lines 20-27. Figures 1-2);

(8) wherein the substrate comprises a group III-V element (see column 13, lines 28-30);

(9) wherein the substrate comprises gallium arsenide (see column 13, lines 28-30);

(11) wherein the plurality of integrated circuits can be interconnected to form a plurality of functional blocks which can be interconnected to create an operational electronic device (see Figures 1-2).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The Rejections

Claims 4-6 and 12-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashisaka (U.S. 5,030,852) in view of Newman et al. (U.S. 5,705,940).

Higashisaka teaches everything above except for the second block connect to form an analog to digital converter; wherein the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC); wherein each of said PHEMT transistors comprises a recess defined in said substrate and a gate formed in said recess; wherein a pinch off voltage of the depletion-mode PHEMT transistor is about positive 0.1 volts. However, Newman discloses a transmit/receive module with **(4)** a. an analog input for electrical signals in communication with at least one of the first block, the second block and the third block; b: a clock input in communication with at least one of the first block, the second block; c: a digital output in communication with at least one of the first block, the second block; d: wherein the first block, the second block connect to form an analog to digital converter (see column 7, lines 39-62); **(5)** wherein the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC) (see column 7, lines 55-58); **(6)** wherein the circuit is a circuit capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies (see column 2, lines 30-34); **(12)** wherein each of said PHEMT transistors comprises a recess defined in said substrate and a gate formed in said recess (see column 18, lines 41-67. Figures 23-24); **(13)** wherein the recess of the depletion mode PHEMT transistor is a single recess (see column 18, lines 41-67. Figures 23-24); **(15)** wherein the recess of the enhancement mode PHEMT transistor is a single recess (see

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column 18, lines 41-67. Figures 23-24); **(16)** wherein the recess of the depletion mode PHEMT transistor is a single recess, and each of said recesses is defined through at least one common layer of said substrate (see column 18, lines 41-67. Figures 23-24); **(17)** wherein at least one of said gates is a T-gate (see Figure 1); **(18)** wherein a pinch off voltage of the depletion-mode PHEMT transistor is about positive 0.1 volts (see column 15, lines 30-45); **(19)** wherein a pinch off voltage of the enhancement-mode PHEMT transistor is about negative 1.0 volts (see column 5, lines 30-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Higashisaka (accordance with the teaching of Newman) to form a transistor since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. Doing so would facilitate the manufacture of the semiconductor device and enhance the performance of the transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong Anh Luu
Patent Examiner
March 24, 2006